A 6GHz-25W GaAs MESFET with an Experimentally Optimized Pattern

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Abstract

A high power GaAs MESFET with a high packing density has been developed by optimizing the gate finger width. The developed power MESFET is the crossover structure and has a total gate width of 15 mm in a 2.2 mm wide chip. The output powers of 25 W at 6 GHz and 20 W at 8 GHz were obtained with 3 dB associated gain from the internally matched four chip devices.

Introduction

A remarkable progress has been made on power GaAs MESFETs in these several years, and 6 GHz-15 W output power has been already obtained [1] [2]. In order to increase the output power furthermore, the total gate width as well as the drain breakdown voltage must be increased. One of the factors limiting the total gate width is the packing density (gate width per unit chip width), because too much increase of the chip width makes the input and output phase nonuniformity serious. The physical device width is also limited in practical devices. Therefore, in order to increase the output power furthermore, it is necessary to develop a new pattern chip with a higher packing density but without deterioration of the power gain and the the thermal resistance.

One of the methods of increasing the packing density is to increase the gate finger width (unit gate width). But the theoretical analysis [3],[4] suggested a serious degradation of the gain due to increase of the gate finger width. In order to obtain the maximum gate finger width in which degradation of the power gain is tolerable, deterioration of the power gain due to increase of the gate finger width was experimentally investigated. It was found that the gate finger width can be increased to more than 200 μm for C-band devices, and the packing density can be increased almost proportionally to the gate finger width without serious gain or thermal resistance deterioration.

According to these experimental results, a new power GaAs MESFET with 15 mm total gate width on a 2.2 mm wide chip was developed. An internally matched four-chip device with 60 mm gate width delivered 25 W at 6 GHz and 20 W at 8 GHz.

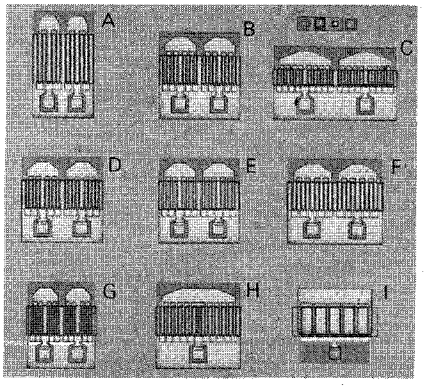

Fig.1 Photograph of the test pattern devices investigated in this work.

Optimized device pattern

In order to find an optimized device pattern, nine test pattern devices with different dimensions and with the same total gate width (3 mm) as shown in Fig.1 were fabricated on a same GaAs wafer in a same run. The crossover structure was adopted for these test pattern devices from the practical point of view. Of these nine test pattern samples, the devices with different gate finger widths (85 μm to 250 μm: sample A. B. C.) and with different gate-to-gate spacings (14 μm to 22 μm: B. F. G.) were used for pattern optimization here.

Figure 2 shows dependence of the microwave performance (linear gain G_L, output power P_o, power added efficiency η_{add}) on the gate finger width at 6 and 8 GHz. There is no explicit degradation of the microwave performance due to increase of the gate finger width until about 250 μm at 6 GHz and 200 μm at 8 GHz. These results indicate that the gate finger width can be increased to twice of that of the previously reported one [2] without any deterioration of the microwave performance, therefore, the chip width can be reduced significantly for the same total gate width device.

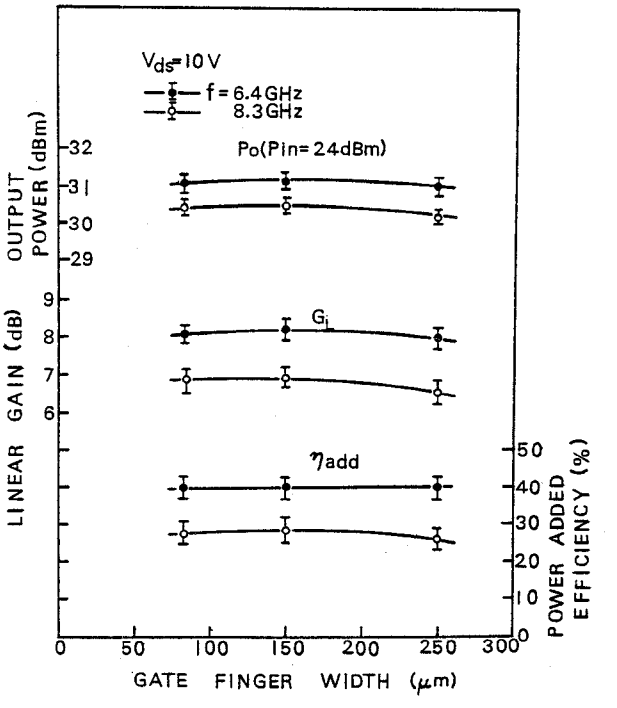

Fig.2 Linear gain G_L, output power P_o and power added efficiency η_{add} at 6.4 GHz and at 8.3 GHz against the gate finger width.

Thermal resistance of the device with interdigitated gates depends on the gate finger width as well as the gate-to-gate spacing. Therefore, when the gate finger width is increased, the gate-to-gate spacing should be changed in order to maintain the same thermal resistance. In order to know the necessary increase of the spacing, the thermal resistance of the test devices with different gate-to-gate spacings and with different gate finger widths was measured using an infrared microscope. The experimental results indicated that the increase in the thermal resistance (24° C/W→27° C/W for 3 mm gate device) due to the increase in the gate finger width (100 μm→200 μm) was cancelled by increasing the spacing from 20 μm to 25 μm.

The top view of the high power GaAs FET chip developed by these experimental design considerations is shown in Fig. 3. The total gate width is designed to be 15 mm so that more than 6 W can be obtained at 6 GHz. The gate finger width is adopted to be 190 μm in order to obtain enough gain up to 8 GHz. The basic FET structure is the graded recess structure which can give a high drain breakdown voltage as well as a high gain [2]. The gate-to-gate spacing, which is determined so that the thermal resistance is 5° C/W, is 25 μm. The chip size is 0.7 mm x 2.2 mm x 0.12 mm. The chip width was reduced to about a half of that of the previously reported decice with 100 μm gate finger width [2] for the same total gate width.

Microwave Performance

The internal matching technique [1] was applied to characterize the microwave performance of one, two and four-chip devices. The equivalent circuit and a photograph of the four chip GaAs FET with the internal watching network is shown in Fig. 4. The input internal matching network consists of two section low pass filter type transformer with lumped elements, and the output matching network is one section semi-distributed form. Although the total gate width of 60 mm is almost twice of the previously reported device [1] [2], the width of the internally matched four chip device is the same as the previous device because of the higher packing density of the new device. This device width (10 mm) is almost physical limit of the practical internally matched device as it is can be seen in Fig. 4.

The output powers and the power added efficiencies of one-, two- and four-chip devices are shown in Fig. 5 as a function of the input power for different drain bias voltages. The one-chip device delivered an output power of about 7 W (4 dB gain) with the power added efficiency of 27 % at 6 GHz, as it is designed. The two-chip device gives more than 10 W with an associated gain of 4 dB at 6 GHz. This result suggests that C-band 10 W power FET has become practical because assembling of two chips in one package is not difficult in production. The internally matched four-chip device with 60 mm gate width gave output powers of 23 W (4 dB gain) or 25 W (3 dB gain) with the maximum power added efficiency of 23 % at 6 GHz band. A four-chip device made

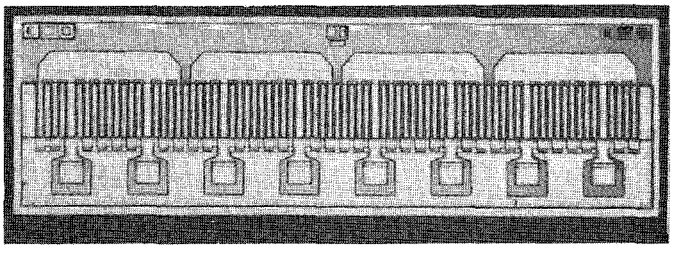

Fig.3 Top view of the new high power GaAs FET chip with 15 mm gate width. Chip size is 0.7 mm x 2.2 mm.

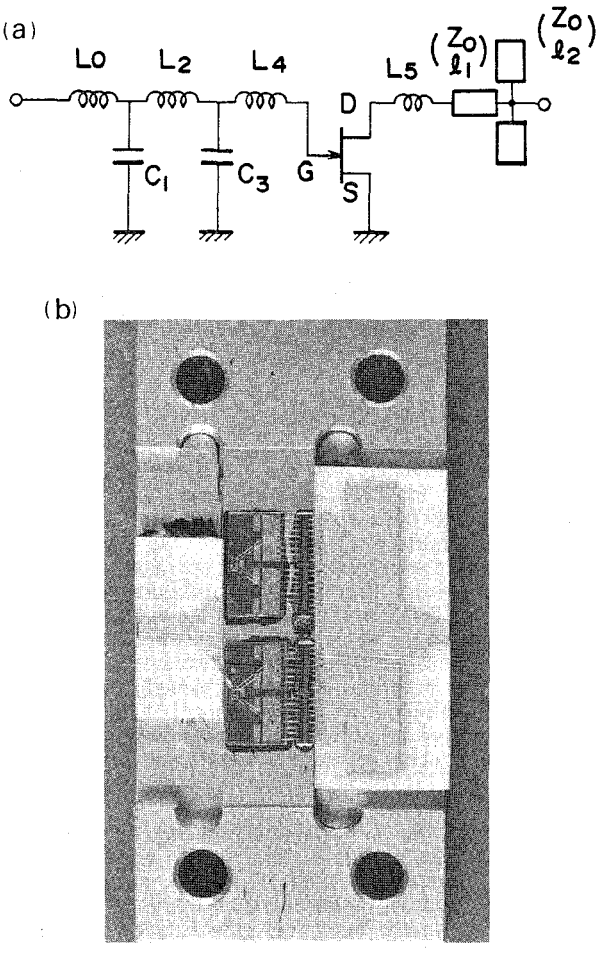

Fig.4 Equivalent circuit of internally matched GaAs MESFET(a), and a photograph of a internally matched four chip device(b).

from the different lot with a slightly shorter gate length (1.0 μm) delivered 20 W power output with an associated gain of 3 dB.

Linear gains and output powers at 6 GHz of the newly developed devices as well as the previously reported devices (gate finger width 100 μm) are plotted against the total gate width in Fig. 6. The output powers of the new devices follow the line obtained on the devices with 100 μm gate finger width, and are almost proportional to the total gate width, indicating no saturation. The linear gain decreases slowly with increase of the total gate width, and seems to saturate instead of dropping rapidly at large gate width region. There is no difference in this tendency between the devices with different gate finger widths. These results indicate that there is negligible deterioration of the microwave performance due to increase of the gate finger width from 100 μm to 190 μm, and that a higher output power can be expected by increasing the total gate width as far as the proper matching circuit are provided.

Figure 7 shows the frequency response of the two-chip and four-chip devices with the internal matching network at 6 GHz (one stage amplifier). A frequency band width of about 1 GHz (5.5-6.5 GHz) is obtained without any external matching.

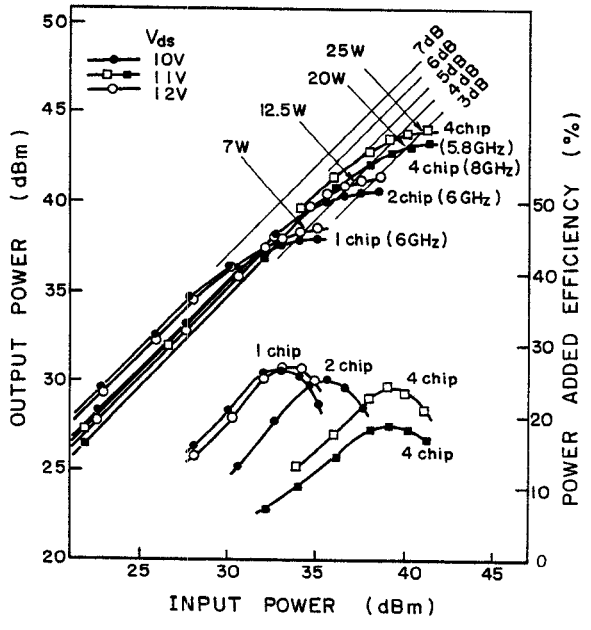

Fig.5 Output powers and power added efficiencies of the internally matched one, two and four chip devices.

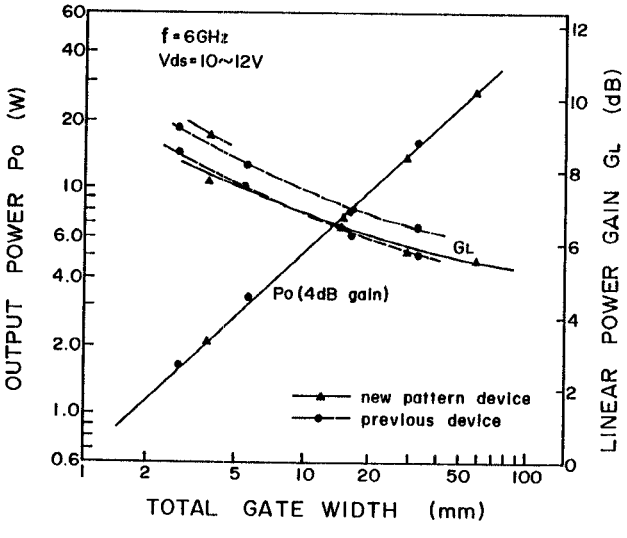

Fig.6 Linear gain and output power against the total gate width.

The temparature rise of the device under operation was also measured by using an infrared microscope. It was confirmed that the temperature rise is about 65°C for a drain bias voltage of 12 V, which is low enough from a view point of device reliability.

Conclusion

Optimization of power GaAs MESFET was brought about by investigating experimentally the dependence of the microwave performance on the gate finger width, and of the thermal resistance on the gate-to-gate spacing. From the experimental results, a new high power GaAs MESFET with a high packing density, having 15 mm-total gate width in a 2.2 mm wide chip, was developed. The internally matched power devices with 60 mm-total gate width were built up on one chip carrier, exhibiting output powers of 25 W at 6 GHz band and 20 W at 8 GHz band with 3 dB associated gain.

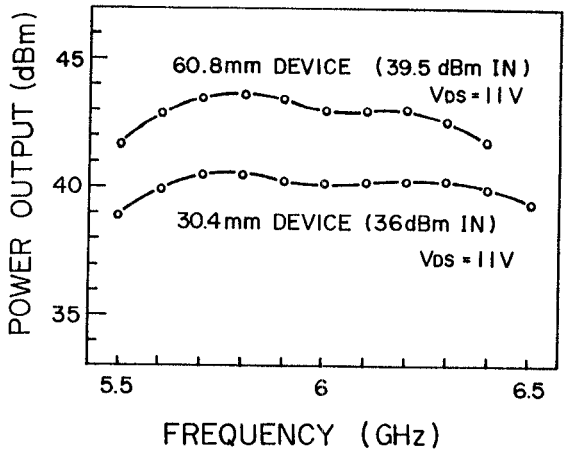

Fig.7 Output power response versus frequency of the internally matched two and four chip devices, measured without any external matching.

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